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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,175	01/16/2004	Yoshihiro Taniguchi	9319S-000626	3256

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EXAMINER	
BRYANT, DELORIS S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,175	TANIGUCHI, YOSHIHIRO	
	Examiner	Art Unit	
	Deloris Bryant	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-8 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita (US 5,473,186) in view of Karasawa et al (US 6,747,322). Morita discloses a semiconductor device comprising: a semiconductor layer (Fig. 3, 21) which contains an element isolation region (Fig. 2; col. 6, lns 55-56) and adjacent doped layers (Fig. 5, 58) isolated from each other by the element isolation region (Fig. 2), wherein a depth X (Fig. 3, 'X' represented by d1', d2', d3') of the element isolation region (Fig. 2) and a width Y (Fig. 3, 'Y' represented by W1, W2, W3) of the element isolation region satisfy an equation represented by X/Y = 1.33 to 1.67 (See Fig. 11-Fig. 12). However, Morita fails to disclose a gate connection layer formed over the element isolation region and

the adjacent doped layers. Karasawa does teach a gate connection layer (Fig. 7; 20 and 22) formed over the element isolation region and the adjacent doped layers (col. 4, lns. 19-55). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the gate connection layer of Karasawa with the teachings of Morita in order to form the first and second driver transistors Q3 and Q4, respectively.

3. Regarding claims 2 and 11, Morita further discloses a semiconductor device wherein the depth of the element isolation region (Fig. 2; col. 6, lns 55-56) is in a range of 0.32 to 0.40 μm (Fig. 8-Fig. 12).

4. Regarding claims 3 and 12, Morita further discloses a semiconductor device wherein the element isolation region (Fig. 2; col. 6, lns 55-56) further comprises a trench element isolation region (Fig. 3, 341, 342, 343).

5. Regarding claims 4 and 13, Morita further discloses a semiconductor device wherein the element isolation region (Fig. 2; col. 6, lns 55-56) comprises a trench (Fig. 3, 341, 342, 343) formed in the semiconductor layer (Fig. 3, 21) and an insulating layer (Fig. 4, 45) provided in the trench (Fig. 3, 341, 342, 343).

6. Regarding claims 5-7, the limitation "an HDP-CVD" (claim 5), "a TEOS plasma CVD" (claim 6), and "SOG" (claim 7) is drawn to a process by which the product is made. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Marosi et al., 218 USPQ 289; and particularly In re

Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

7. Regarding claims 8 and 14, Morita further discloses a semiconductor device wherein the adjacent doped layers (Fig. 1E, 8) further comprises two doped layers having the same conductivity (Fig. 1E).

8. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita (US 5,473,186) in view of Karasawa et al (US 6,747,322) and in further view of Liaw et al (US 5,955,768). Morita and Karasawa discloses limitations set forth in claims 1 and 10 except neither Morita nor Karasawa disclose two doped layers with the same conductivity, which is contained in respective memory cells adjacent to each other. Liaw does teach two doped layers (Fig. 2I, 35B, 35C) contained in respective memory cells adjacent to each other (see Fig. 2I). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have memory cells, which contain doped layers adjacent to each other. One would have been motivated to so modify Morita and Karasawa with that of Liaw to minimize size and provide minimum resistance in the source/drain region (col. 4, lns 21-35).

Response to Arguments

9. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-8670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dsb

CARL WHITEHEAD, JR.
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